Improvement of SGP modelling using additional devices

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2009 October 22th

Motivation

- NXP small signal bipolar transistors are modeled by using Standard Gummel Poon (SGP) model
- Some models offered to customers are old and no more accurate (e.g. by redesign of die)
- Revision of these models
- SGP very simple model compared with HICUM etc. but:

Motivation

- Many customers like SGP model because of its properties:
  - simple model
  - cheap and simple simulators (e.g. PSpice etc.) available

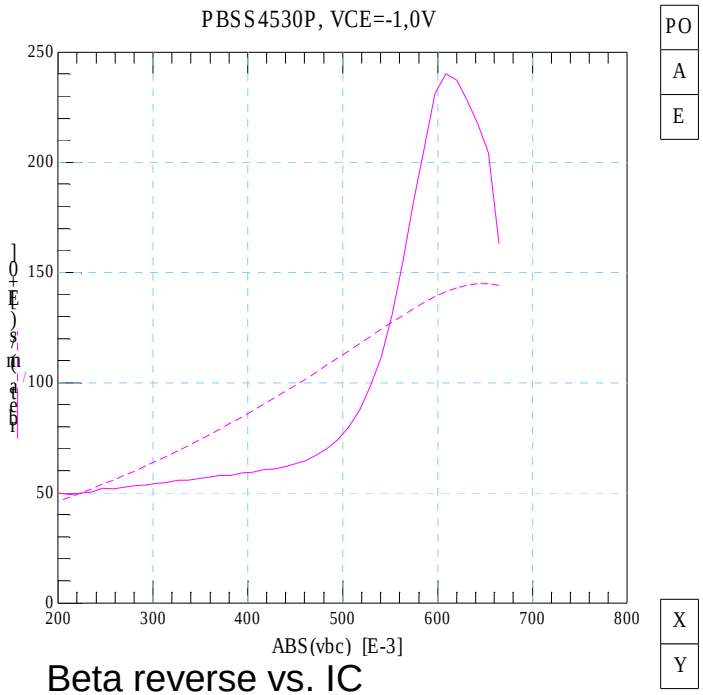
- For many small signal transistors SGP model is sufficient

- Some disadvantages, especially poor fitting in some kinds of operation

- Misfitting often occurs when modelling transistors with higher VCEO (typically with VCEO > 40V)

Modelling problem (1)

- Modelling the BF Slope without additional devices is difficult
- Poor fitting of reverse BF is hampering forward modelling

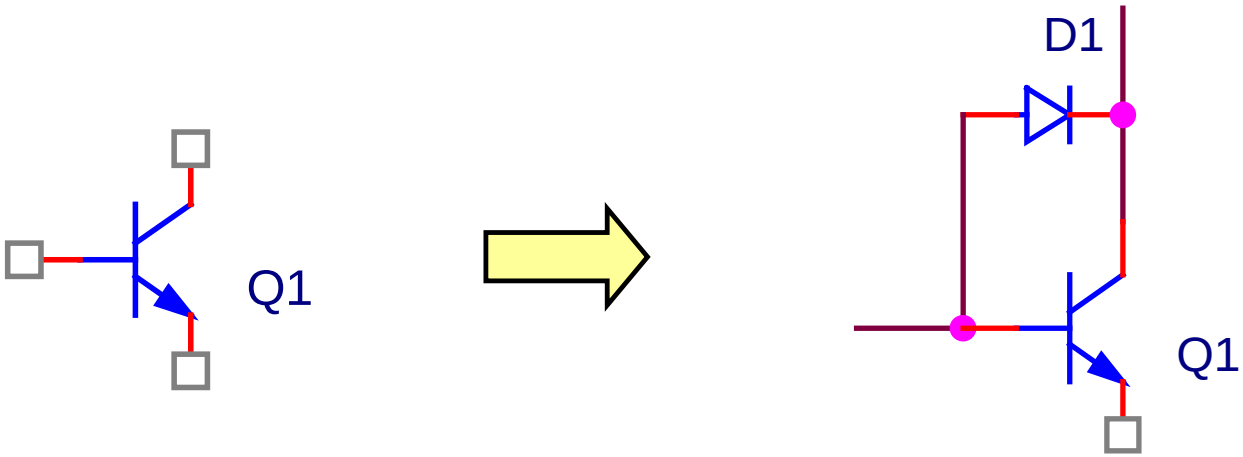


Beta reverse vs. IC

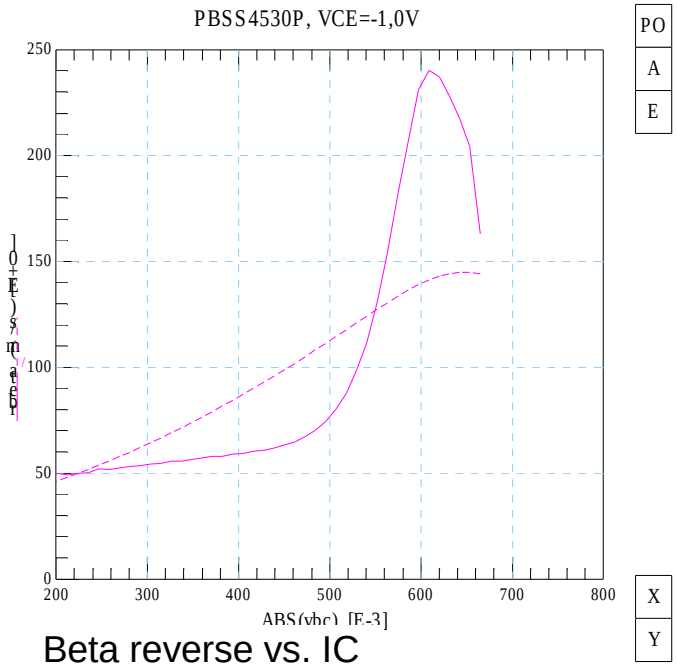
Solid line: measured data
Dashed line: simulated data

Improvement of reverse modelling

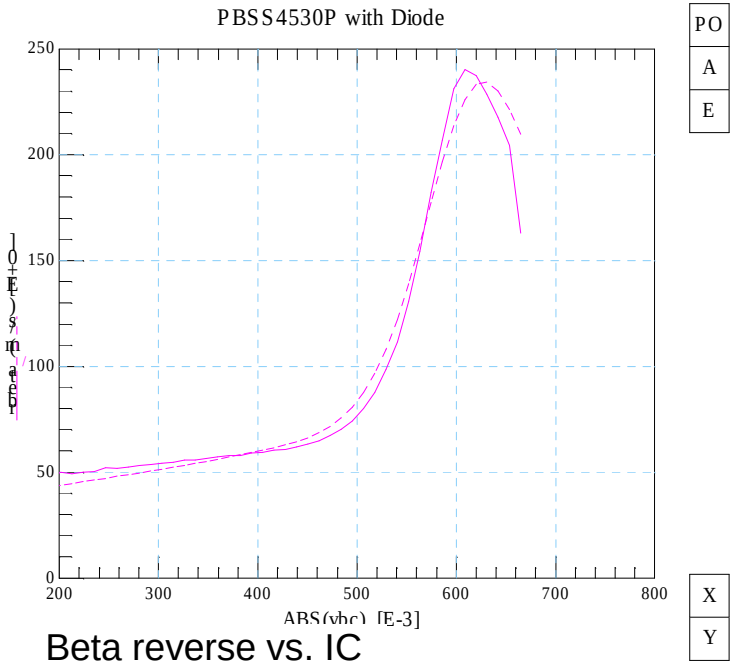
- Use of a additional diode parallel to the B-C junction of the transistor in conducting direction



Improvement of reverse modelling



Beta reverse vs. IC



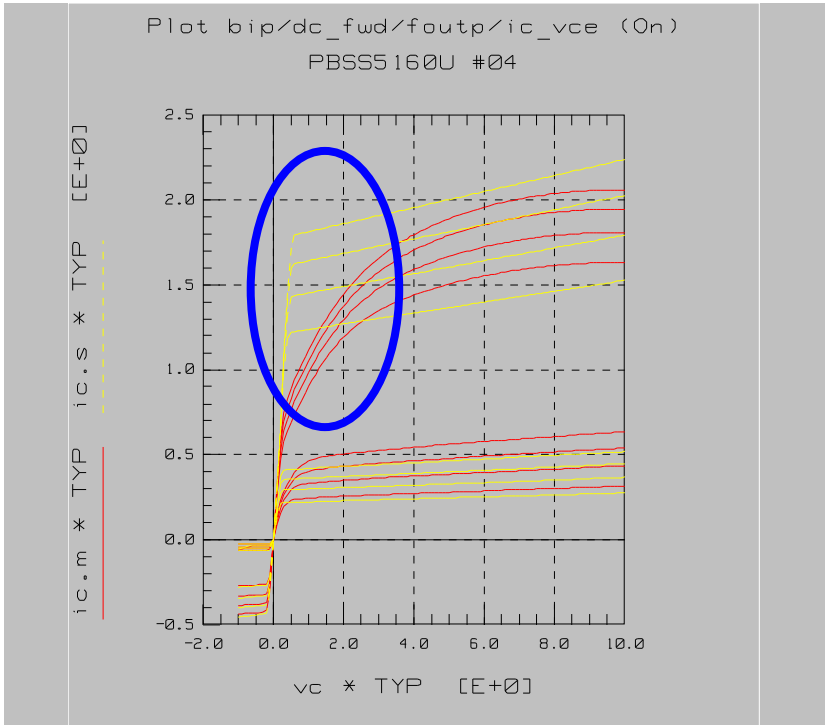
Beta reverse vs. IC

- Result: Good fitting in reverse mode of operation
- Facilitation of modeling in forward direction

Modelling problem (2)

- SGP-Model is not able to calculate area of quasisaturation accurately
- No smooth change, only sharp bend
- Poor fitting in this area

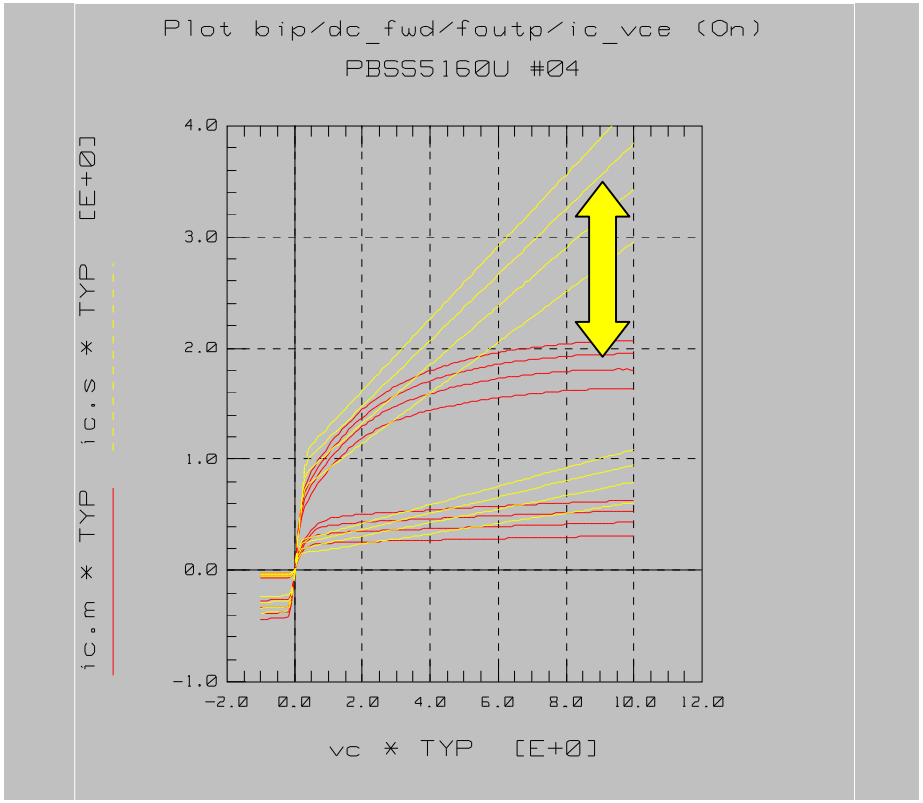
Red line : measured data
Yellow line: simulated data



output characteristic (VC vs. IC)

Modelling up to now

- Decreasing of VAF (and IKF) to archive better fitting of quasi saturation
- Possible solution for low-VCEsat-transistors, but poor fitting in area of linear operation!

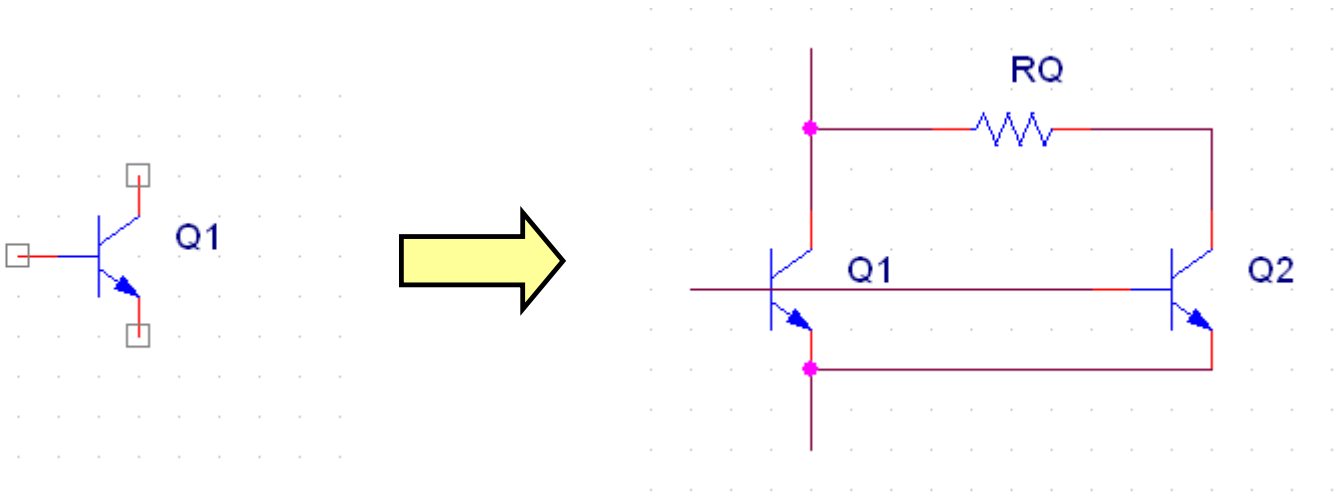


output characteristic (VC vs. IC)

Red line : measured data
Yellow line: simulated data

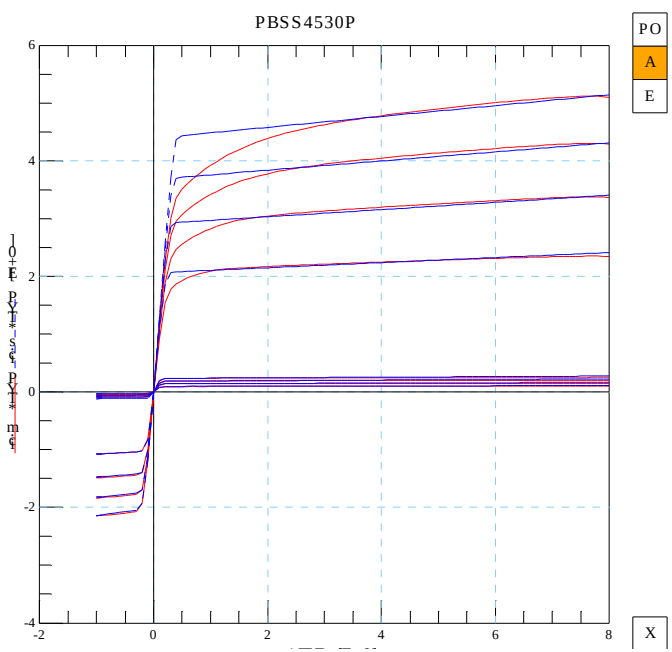
Improvement of quasi saturation

- Use of a second transistor (Q2) with resistor (RQ) parallel to the main transistor (Q1)

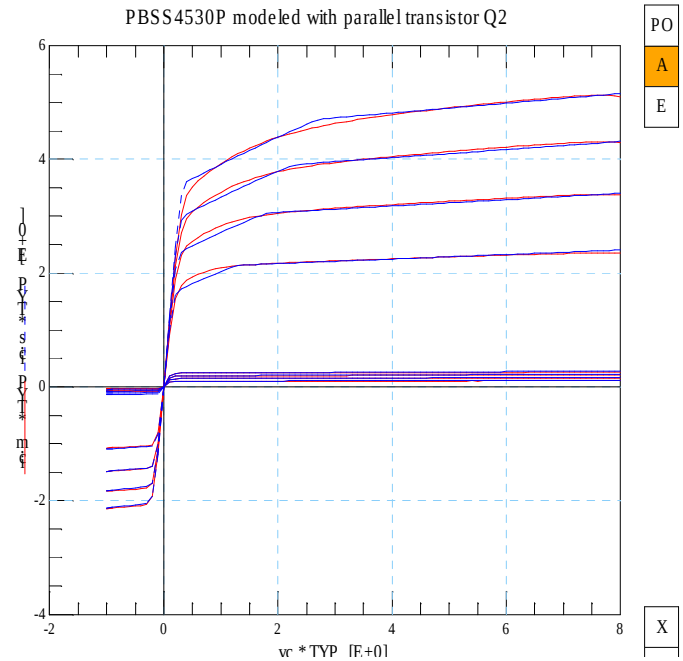


Improvement of quasi saturation

- Modelling result with parallel transistor Q2:



output characteristic (VC vs. IC)

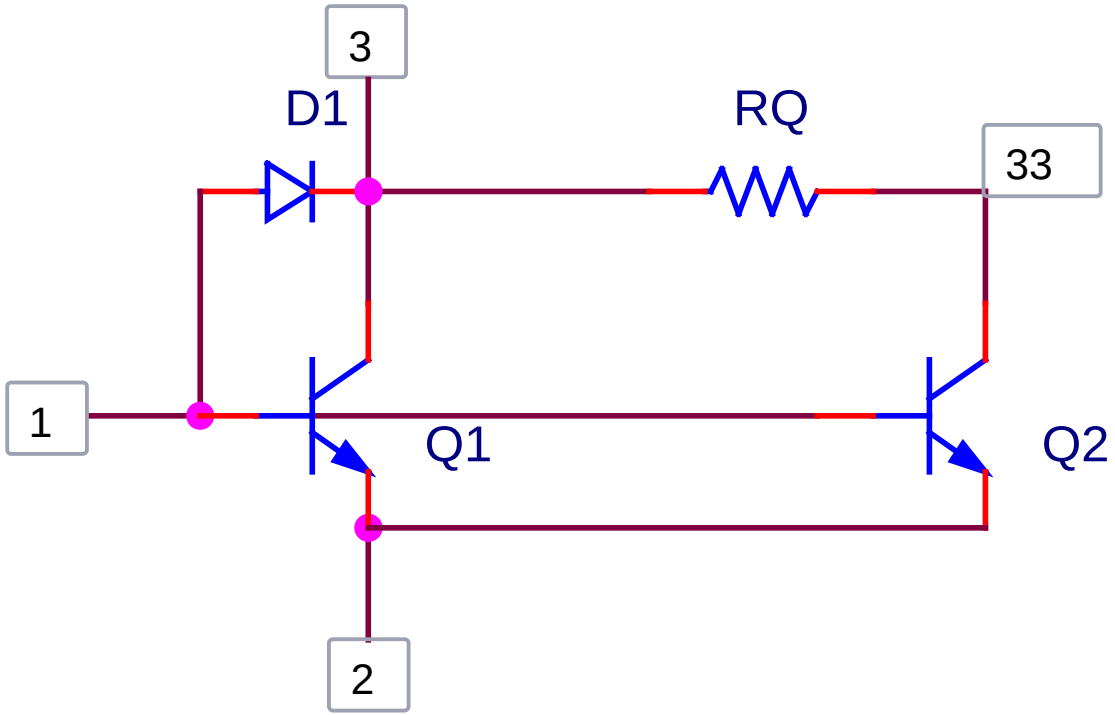


output characteristic (VC vs. IC)

Red line : measured data
Blue line: simulated data

Example for enhanced model

- .SUBCKT PBSS4612PA 3 1 2
- *
- Q1 3 1 2 MAIN
- + Area = 0.9871
- Q2 33 1 2 MAIN
- + Area = 0.0129
- D1 1 3 DIODE
- RCQ 3 33 11.23
- *
- *
- .MODEL MAIN NPN
- + IS = 3.467E-012
- + NF = 0.9647
- + etc.
- *
- *
- .MODEL DIODE D
- + IS = 1.313E-014
- + N = 1.01
- + etc...
- .ENDS



- Ratio of Q1 and Q2 is determined by the variable "Area"

Difficulties

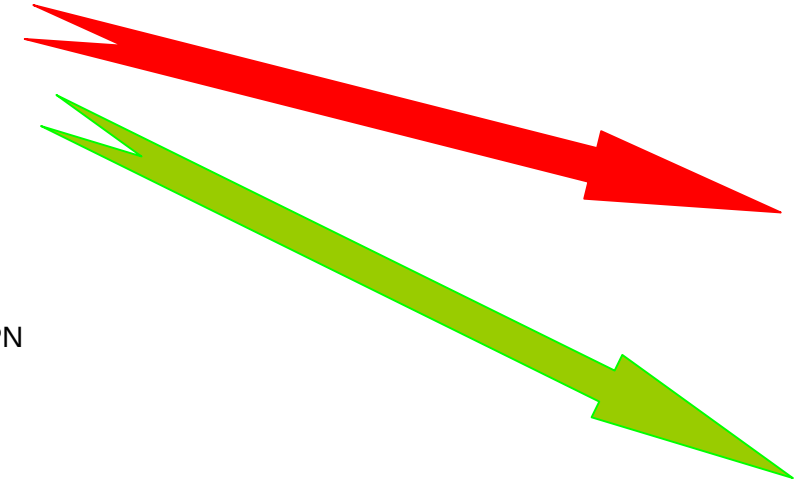
- Some simulators (e.g. PSpice student) do no accept the variable “Area”
- Possible solution: Use of two different transistors with different parameters and “included” area-variable:

- Proceeding:
  - *To be multiplied with area:*
    IS, ISE, ISC, ISS, IKF, IKR, IRB, ITF, CJE, CJC, CJS, QCO
  - *To be divided by area:*
    RE, RC, RB, RBM
  - *All other Parameters stay unchanged*

(Source: Khakzar, ISBN 3-8169-1262-1, page 222)

Parameters for new model

- .SUBCKT PBSS4612PA 3 1 2
- *
- Q1 3 1 2 MAIN
- + Area = 0.9683
- Q2 33 1 2 MAIN
- + Area = 0.03168
- D1 1 3 DIODE
- RCQ 3 33 11.23
- *
- *
- .MODEL MAIN NPN
- + IS = 3.467E-012
- + NF = 0.9647
- + etc.
- *
- *
- .MODEL DIODE D
- + IS = 1.313E-014
- + N = 1.01
- + etc...
- .ENDS



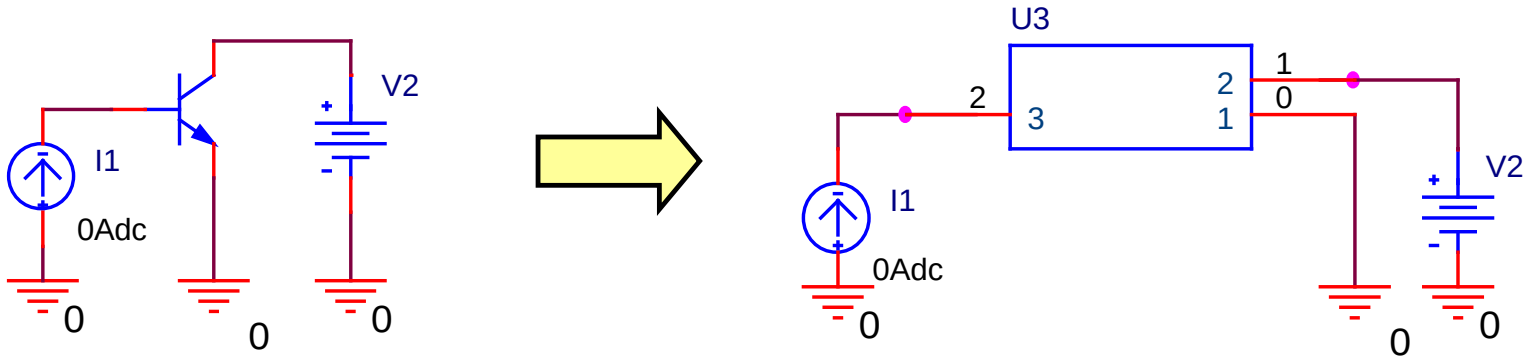
- .SUBCKT PBSS4612PA 3 1 2
- *
- Q1 3 1 2 MAIN
- Q2 33 1 2 SUB
- D1 1 3 DIODE
- RCQ 3 33 11.23
- *
- .MODEL MAIN NPN
- + IS = 3.365E-012
- + NF = 0.9647
- + etc.
- *
- *.MODEL SUB NPN
- + IS = 1.09E-013
- + NF = 0.9647
- + etc.
- *
- .MODEL DIODE D
- + IS = 1.313E-014
- + N = 1.01
- + etc...
- .ENDS

Remarks

- Disadvantage:

  In schematics subcircuits are displayed as black box; the transistor symbol will be lost.

- Possibility of creating an .olb-file, but circumstancial



Summary

- Modelling problems with bipolar transistors with higher VCEO using SGP-model
- Quasi saturation and reverse mode of operation can be improved by inserting additional diode and transistor / resistor
- Necessity of subcircuits
- Higher accuracy of models, but even higher complexity

Remarks

- Experience with such complex models? Most companies are offering simple models without using subcircuits. => reason?
- Difficult to get customer feedback about such matters.
- Acceptance of customers especially concerning confusing schematics?